

Figure 1

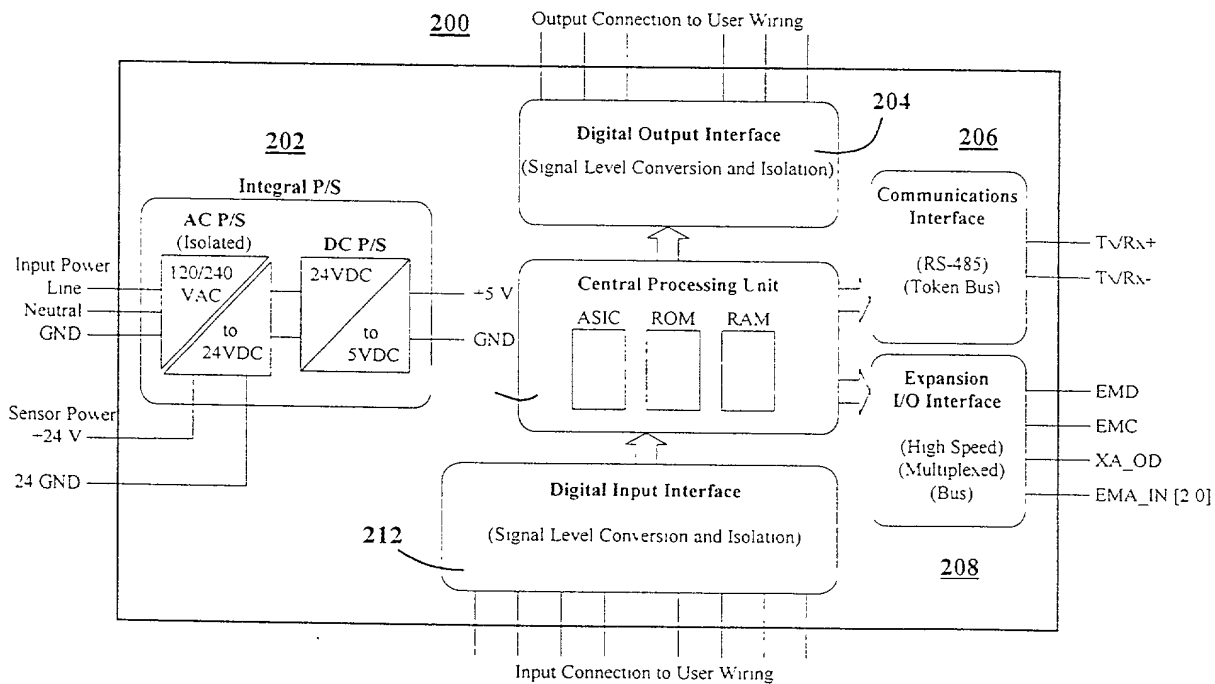


Figure 2

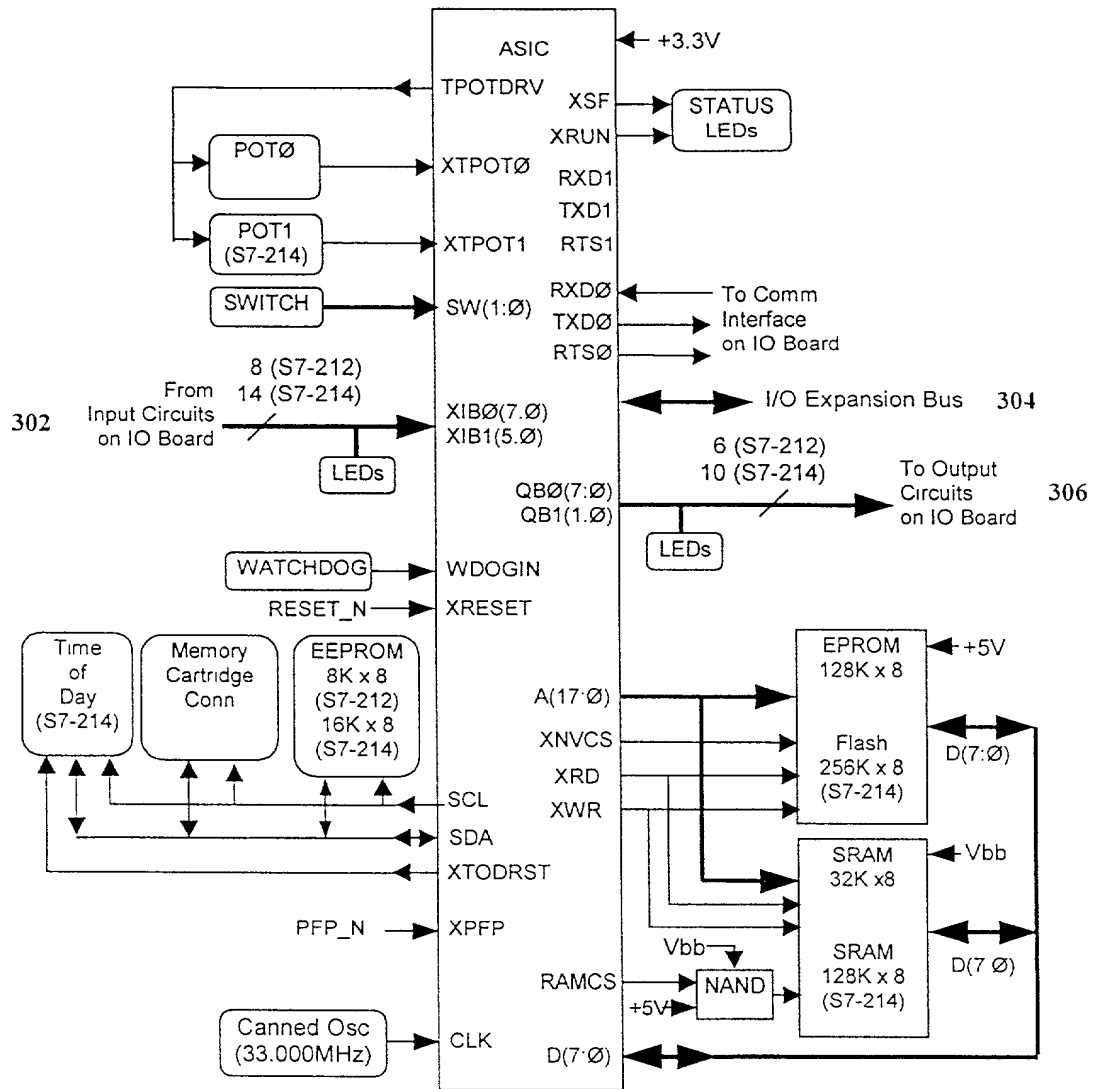


Figure 3

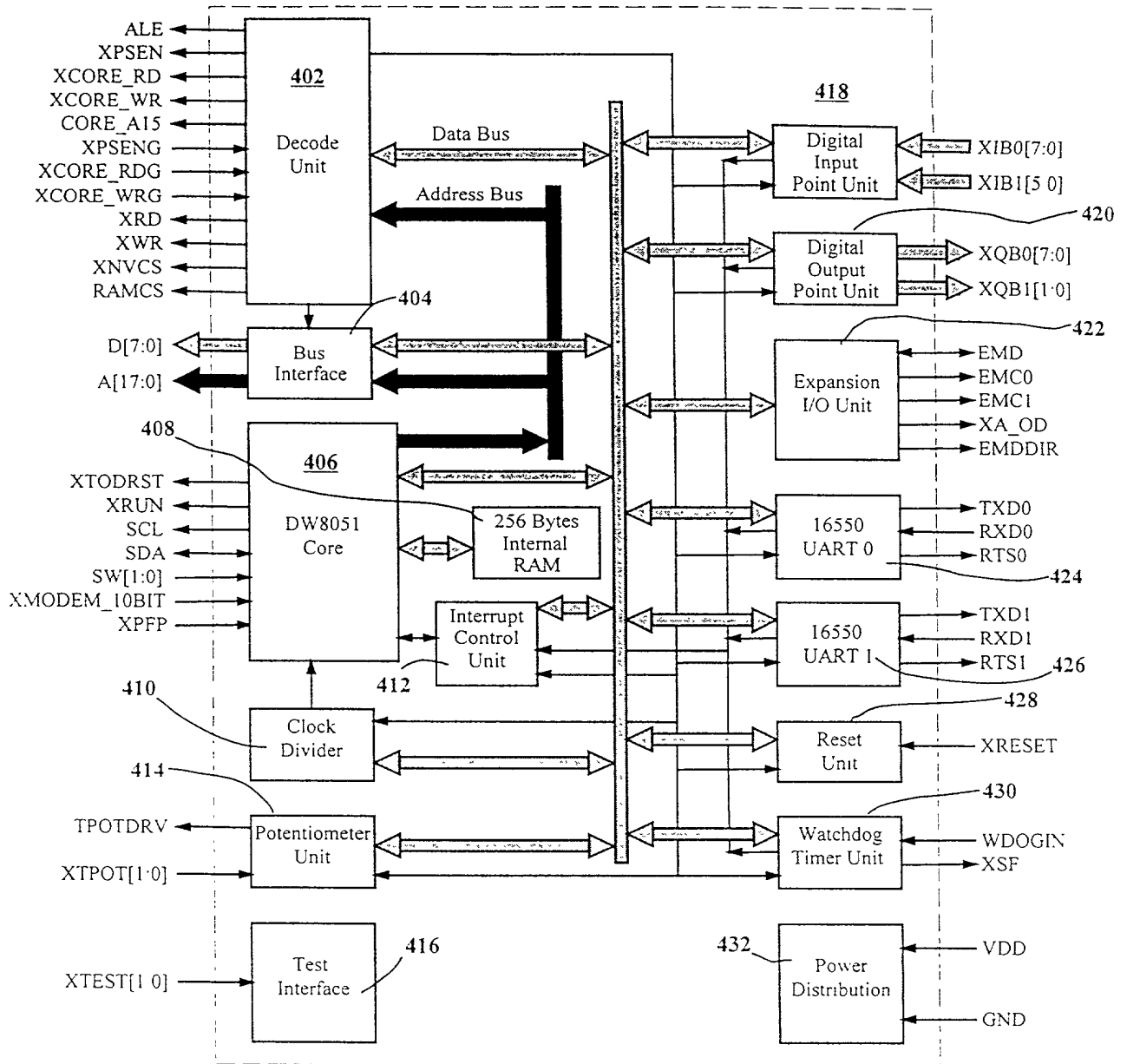


Figure 4

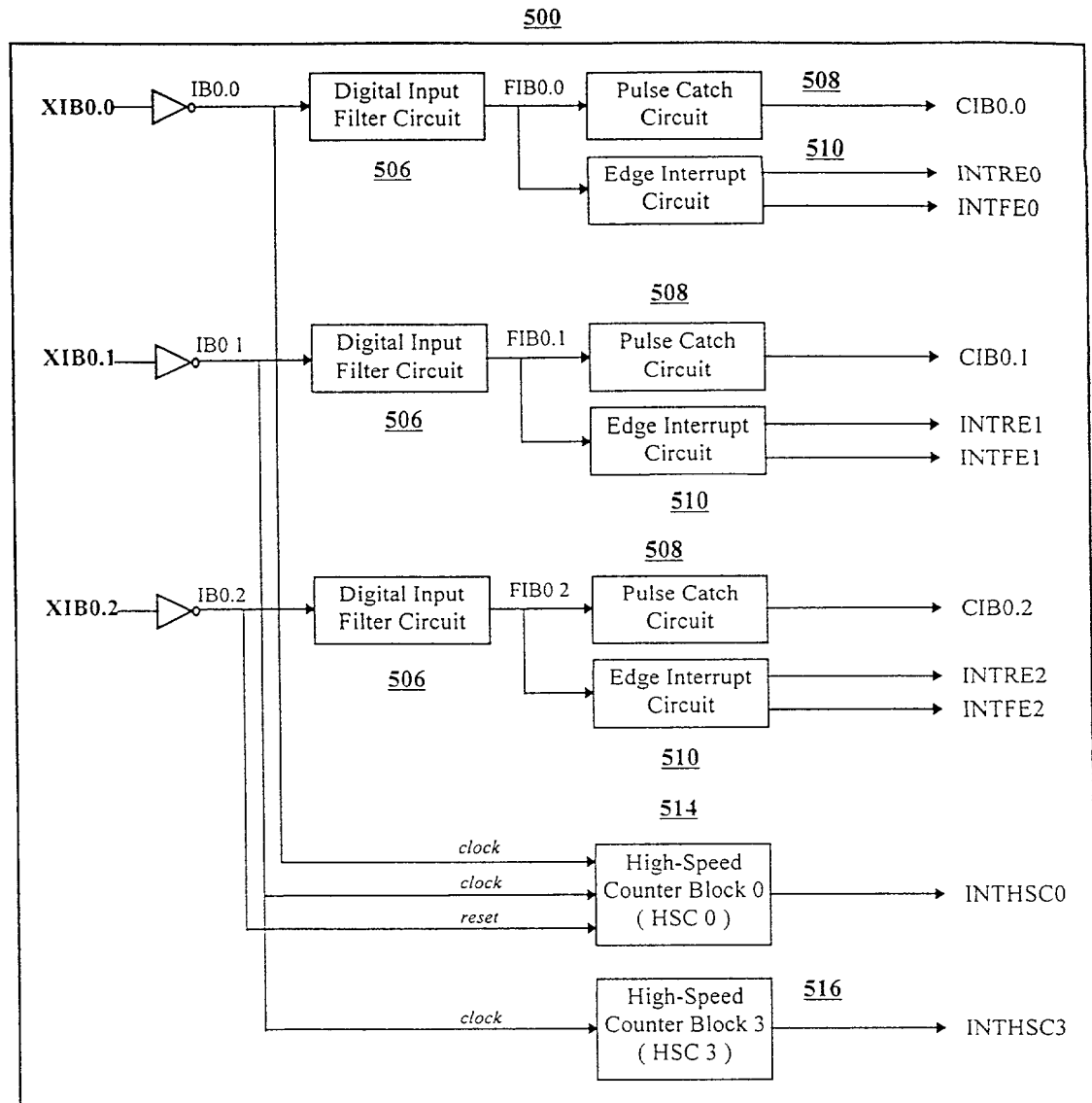


Figure 5

600

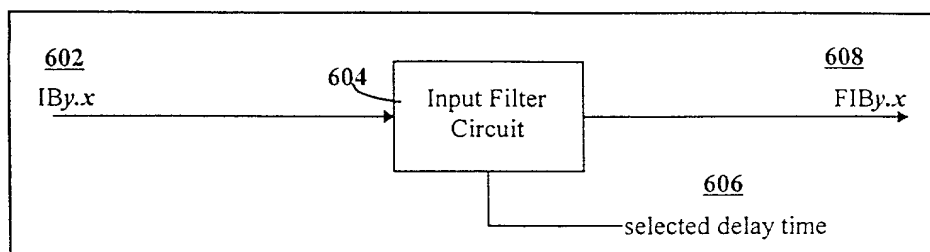


Figure 6a

Digital Filter Operation Definition

Input Point State	Current Count	Next Count	Present Output Value	Next Output Value
0 (decrements counter)	0 n, where $3 \geq n > 0$ 4 n, where $15 \geq n > 4$	0 $n - 1$ 3 $n - 1$	0 0 1 1	0 0 0 1
1 (increments counter)	n, where $11 > n \geq 0$ 11 n, where $14 \geq n > 11$ 15	$n + 1$ 12 $n + 1$ 15	0 0 1 1	0 1 1 1

Figure 6b

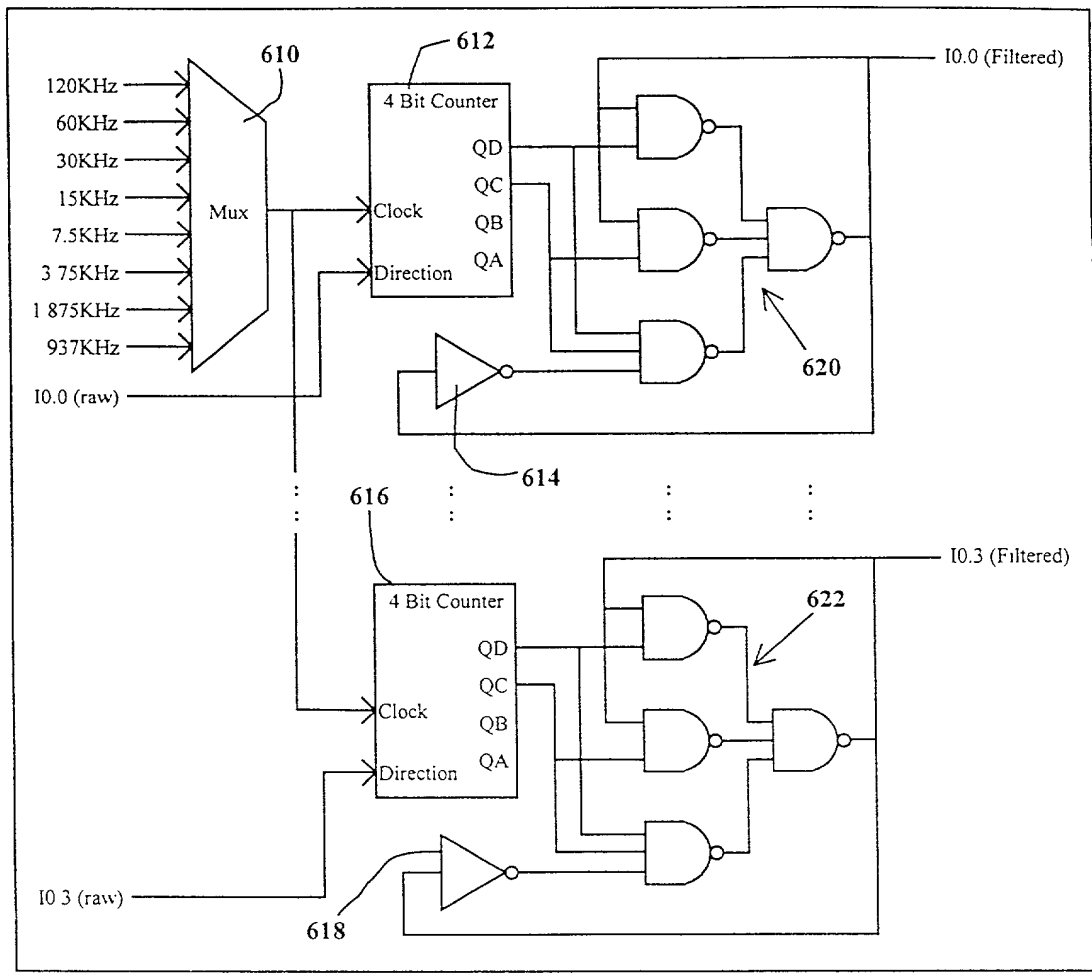


Figure 6c

Frequency	Period	Number of Counts	Delay time
120 KHz	8.33 μ sec	12	0.1 ms
60 KHz	16.6 μ sec	12	0.2 ms
30 KHz	33.3 μ sec	12	0.4 ms
15 KHz	66.7 μ sec	12	0.8 ms
7.5 KHz	133 μ sec	12	1.6 ms
3.75 KHz	267 μ sec	12	3.2 ms
1.875 KHz	533 μ sec	12	6.4 ms
937 KHz	1067 μ sec	12	12.8 ms

Figure 6d

Register Value	Corresponding delay time
00	0.2 ms
01	0.4 ms
02	0.8 ms
03	1.6 ms ¹
04	1.6 ms ¹
05	3.2 ms
06	6.4 ms
07	12.8 ms
08 to FF	no delay

¹ Two selections for 1.6 ms delay time exist for 1st generation ASIC compatibility reasons

Figure 7

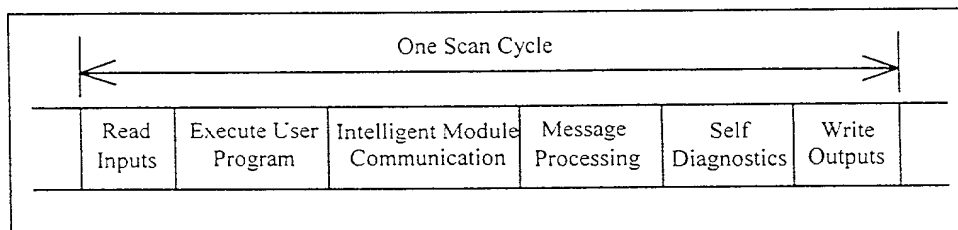


Figure 8

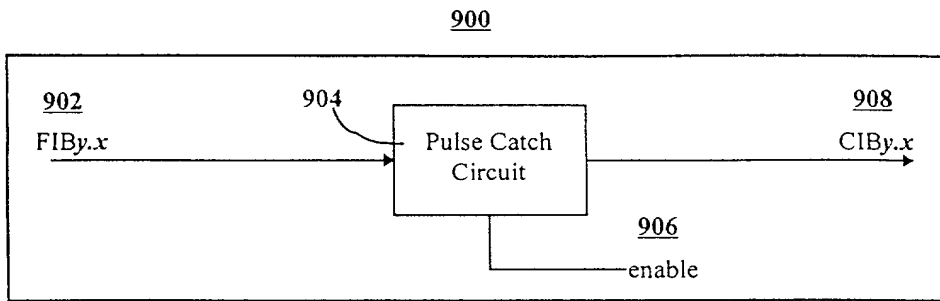


Figure 9

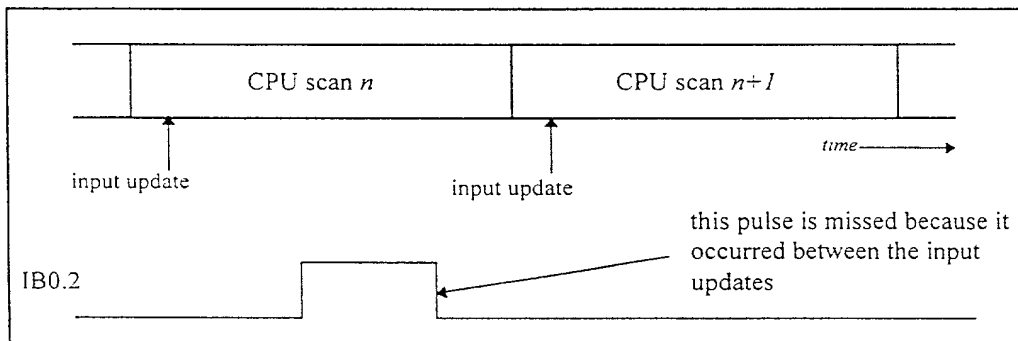


Figure 10

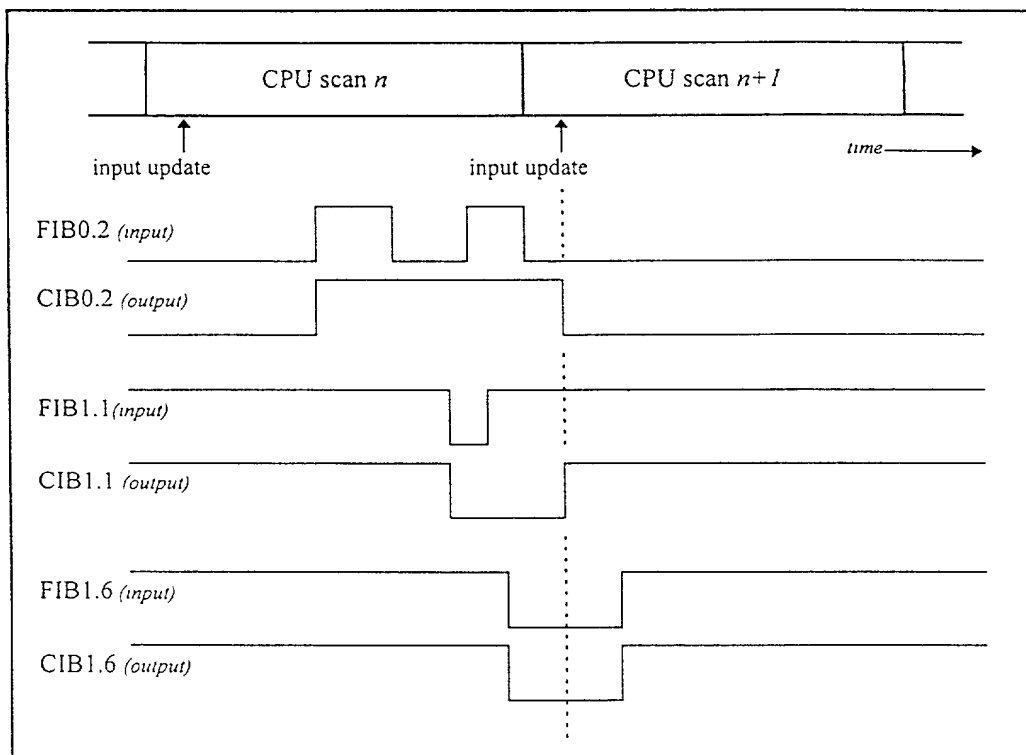


Figure 11

PCE	PS CV	PS F	RP	NS CV	NS F	Comment
1	I	0	-	CV	0	I = CV and F is not set; RP is a don't care
1	not I	0	-	I	1	I ≠ CV; capture new value of I and set F = 1
1	-	1	0	CV	1	CV has not been read
1	-	1	1	I	0	CV has been read; set CV = I
0	-	-	-	I	0	Pulse catch disabled; CV = I

Figure 12a

Pulse Catch Enable Registers															
Address	Description														
0002H	register name: IB0_Pulse_Catch_Enable_Register (IB0PCE) size: byte (8-bit) access: read / write reset value: 00H <div style="text-align: center;"> 70 </div> <table border="1" style="width: 100%; border-collapse: collapse; text-align: center;"> <tr> <td>EN7</td><td>EN6</td><td>EN5</td><td>EN4</td><td>EN3</td><td>EN2</td><td>EN1</td><td>EN0</td></tr> </table> ENx: 1 = enables pulse catch operation on input point IB0.x 0 = disables pulse catch operation on input point IB0.x							EN7	EN6	EN5	EN4	EN3	EN2	EN1	EN0
EN7	EN6	EN5	EN4	EN3	EN2	EN1	EN0								
0003H	register name: IB1_Pulse_Catch_Enable_Register (IB1PCE) size: byte (8-bit) access: read / write reset value: 00H <div style="text-align: center;"> 70 </div> <table border="1" style="width: 100%; border-collapse: collapse; text-align: center;"> <tr> <td>x</td><td>x</td><td>EN5</td><td>EN4</td><td>EN3</td><td>EN2</td><td>EN1</td><td>EN0</td></tr> </table> ENx: 1 = enables pulse catch operation on input point IB1.x 0 = disables pulse catch operation on input point IB1.x							x	x	EN5	EN4	EN3	EN2	EN1	EN0
x	x	EN5	EN4	EN3	EN2	EN1	EN0								

Figure 12b

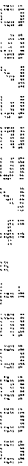
register IB0PS:	Read of this register returns CIB0[7:0] and retriggers pulse catch circuits for IB0 input points	used by SW for input update
register IB1PS:	Read of this register returns CIB1[5:0] and retriggers pulse catch circuits for IB1 input points	used by SW for input update
register IB0PSNR:	Read of this register returns CIB0[7:0] and leaves pulse catch circuits unaffected	used by SW for immediate access
register IB1PSNR:	Read of this register returns CIB1[5:0] and leaves pulse catch circuits unaffected	used by SW for immediate access

Figure 12c

Input Point Status Registers									
Address	Description								
0004H	<div>register name: IB0_Input_Point_Status_Register (IB0PS)</div> <div>size: byte (8-bit)</div> <div>access: read only</div> <div>reset value: 00H</div> <div><div>70</div><table><tr><td>CI7</td><td>CI6</td><td>CI5</td><td>CI4</td><td>CI3</td><td>CI2</td><td>CI1</td><td>CI0</td></tr></table></div> <div>CIx: Contains conditioned input point state CIB0.x</div>	CI7	CI6	CI5	CI4	CI3	CI2	CI1	CI0
CI7	CI6	CI5	CI4	CI3	CI2	CI1	CI0		
0005H	<div>register name: IB1_Input_Point_Status_Register (IB1PS)</div> <div>size: byte (8-bit)</div> <div>access: read only</div> <div>reset value: 00H</div> <div><div>70</div><table><tr><td>x</td><td>x</td><td>CI5</td><td>CI4</td><td>CI3</td><td>CI2</td><td>CI1</td><td>CI0</td></tr></table></div> <div>CIx: Contains conditioned input point state CIB1.x.</div>	x	x	CI5	CI4	CI3	CI2	CI1	CI0
x	x	CI5	CI4	CI3	CI2	CI1	CI0		
0006H	<div>register name: IB0_Input_Point_Status_Register_No_Retrigger (IB0PSNR)</div> <div>size: byte (8-bit)</div> <div>access: read only</div> <div>reset value: 00H</div> <div><div>70</div><table><tr><td>CI7</td><td>CI6</td><td>CI5</td><td>CI4</td><td>CI3</td><td>CI2</td><td>CI1</td><td>CI0</td></tr></table></div> <div>CIx: Contains conditioned input point state CIB0.x</div>	CI7	CI6	CI5	CI4	CI3	CI2	CI1	CI0
CI7	CI6	CI5	CI4	CI3	CI2	CI1	CI0		
0007H	<div>register name: IB1_Input_Point_Status_Register_No_Retrigger (IB1PSNR)</div> <div>size: byte (8-bit)</div> <div>access: read only</div> <div>reset value: 00H</div> <div><div>70</div><table><tr><td>x</td><td>x</td><td>CI5</td><td>CI4</td><td>CI3</td><td>CI2</td><td>CI1</td><td>CI0</td></tr></table></div> <div>CIx: Contains conditioned input point state CIB1.x.</div>	x	x	CI5	CI4	CI3	CI2	CI1	CI0
x	x	CI5	CI4	CI3	CI2	CI1	CI0		

Figure 12d

Variable	Mean	SD	Min	Max
Age	34.5	10.2	21	55
Gender	0.5	0.5	0	1
Marital status	0.6	0.5	0	1
Education	12.5	1.5	9	16
Income	1500	500	500	3000
Health status	0.8	0.2	0	1
Employment status	0.7	0.3	0	1
Family size	3.2	1.1	1	6
Home ownership	0.9	0.1	0	1
Auto ownership	0.6	0.5	0	1
Life satisfaction	4.5	1.2	1	7
Health satisfaction	5.2	1.0	1	7
Income satisfaction	4.8	1.1	1	7
Home satisfaction	5.5	0.9	1	7
Auto satisfaction	5.1	1.0	1	7
Family satisfaction	5.3	1.1	1	7
Life satisfaction (total)	4.5	1.2	1	7
Health satisfaction (total)	5.2	1.0	1	7
Income satisfaction (total)	4.8	1.1	1	7
Home satisfaction (total)	5.5	0.9	1	7
Auto satisfaction (total)	5.1	1.0	1	7
Family satisfaction (total)	5.3	1.1	1	7



Variable	Mean	SD	Min	Max
Age	34.5	10.2	21	55
Gender	0.5	0.5	0	1
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Education	12.5	1.5	9	16
Income	1500	500	500	3000
Health status	0.8	0.2	0	1
Employment status	0.7	0.3	0	1
Family size	3.2	1.1	1	6
Home ownership	0.9	0.1	0	1
Auto ownership	0.6	0.5	0	1
Life satisfaction	4.5	1.2	1	7
Health satisfaction	5.2	1.0	1	7
Income satisfaction	4.8	1.1	1	7
Home satisfaction	5.5	0.9	1	7
Auto satisfaction	5.1	1.0	1	7
Family satisfaction	5.3	1.1	1	7
Life satisfaction (total)	4.5	1.2	1	7
Health satisfaction (total)	5.2	1.0	1	7
Income satisfaction (total)	4.8	1.1	1	7
Home satisfaction (total)	5.5	0.9	1	7
Auto satisfaction (total)	5.1	1.0	1	7
Family satisfaction (total)	5.3	1.1	1	7

1200f

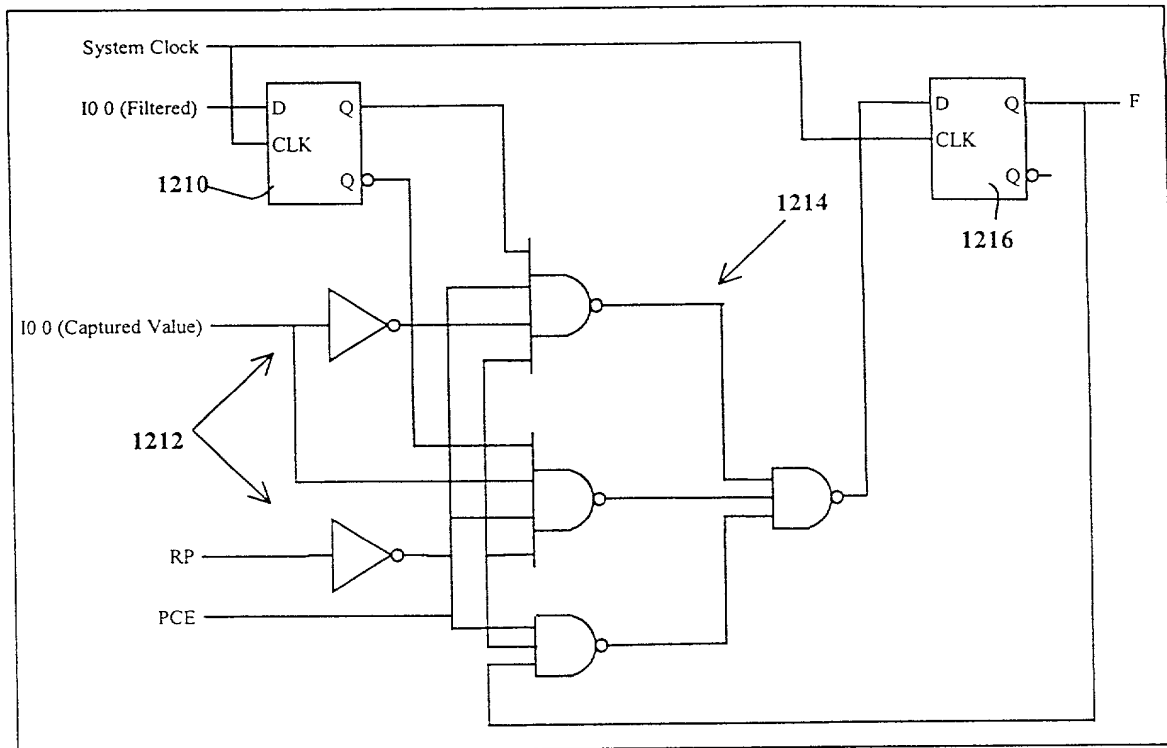


Figure 12f

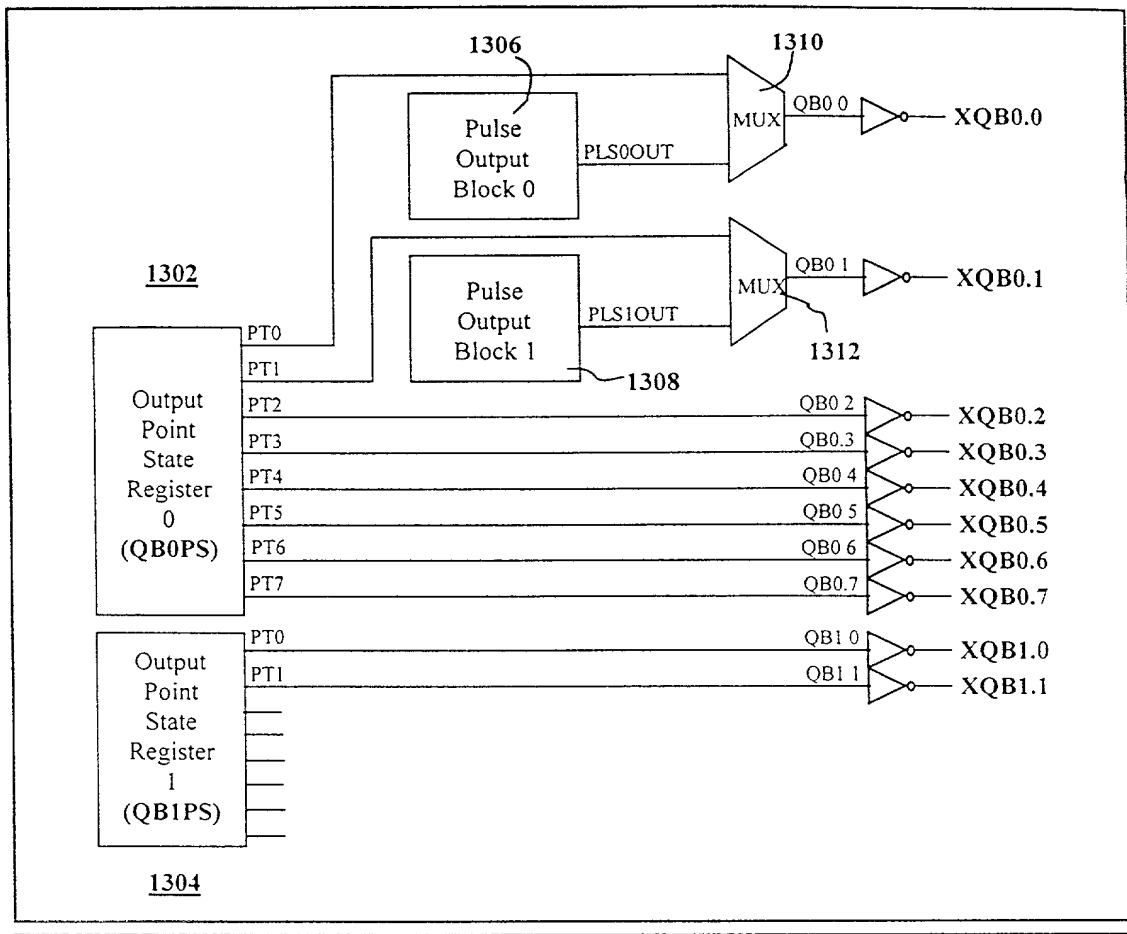


Figure 13

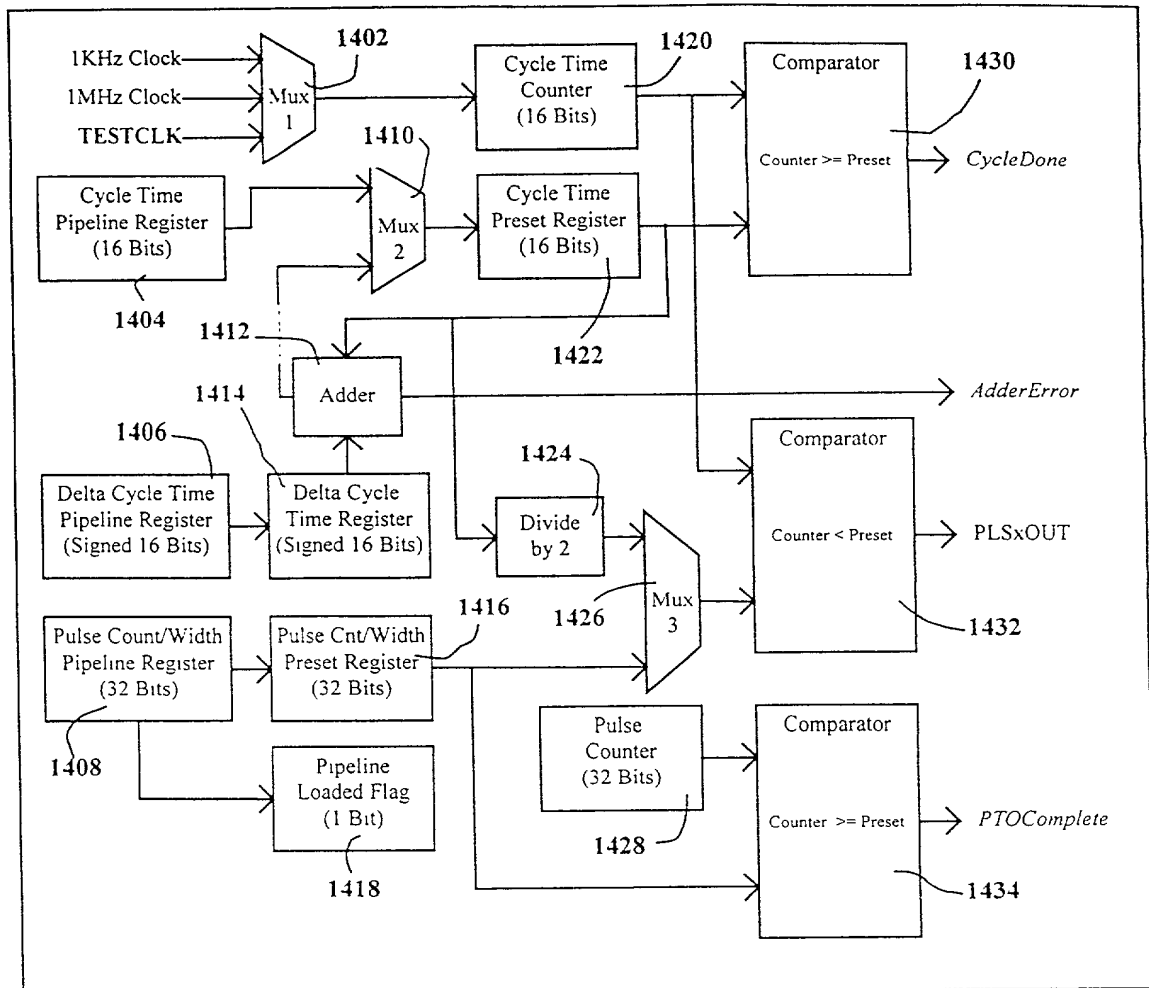


Figure 14a

Register Name	Valid Value Range
Cycle Time Preset Register	2 to 65535
Cycle Time Pipeline Register	
Delta Cycle Time Register	-32768 to 32767
Delta Cycle Pipeline Register	
Pulse Count/Width Preset Register	1 to $(2^{32}-1)$ 0 to 65535
Pulse Count/Width Pipeline Register	PTO mode PWM mode

Figure 14b

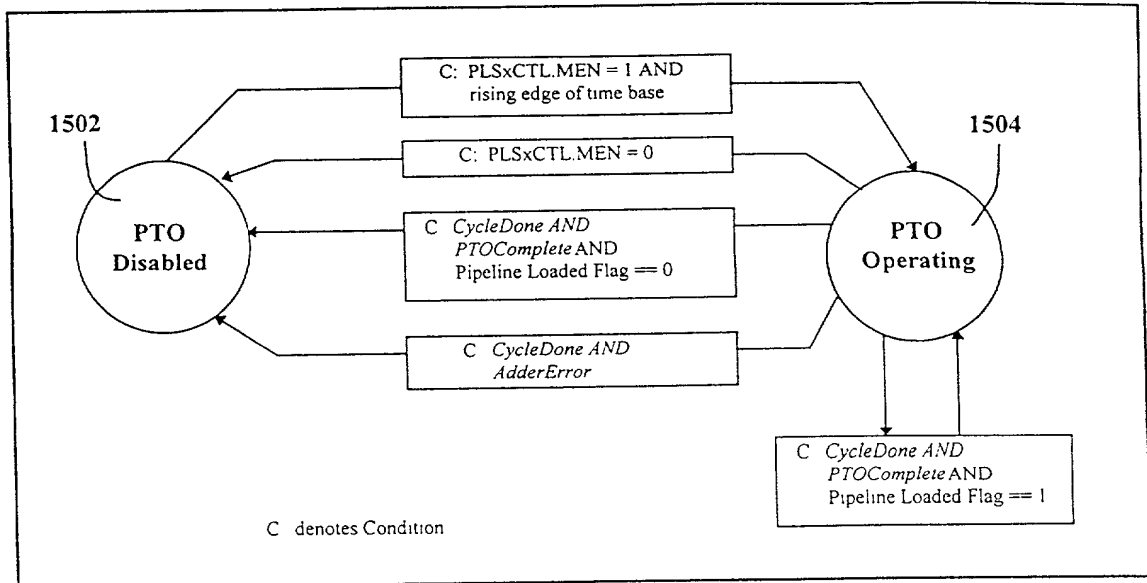


Figure 15

```

cycle time counter = cycle time counter + 1;
IF (cycle time counter >= cycle time preset) THEN
BEGIN // this is the CycleDone event
-----
    pulse counter = pulse counter + 1;
    IF (pulse counter >= pulse count preset) THEN
    BEGIN // this is the PTOComplete event
    -----
        assert INTxPLS signal, if PTOComplete interrupts are enabled:
        IF (pipeline loaded flag is set) THEN
        BEGIN
            -----
            transfer values from pipeline registers into operating registers,
            set pulse counter = 0;
            clear pipeline loaded flag;
            -----
        END
        ELSE // pipeline loaded flag is not set
        BEGIN
            -----
            GOTO PTO Disabled state; // disable the PLS block now
            -----
        END
        ENDIF
    -----
    END
    ELSE // not yet at PTOComplete
    BEGIN
        -----
        cycle time preset = cycle time preset + delta cycle time.
        IF (cycle time preset exceeds bounds) THEN
        BEGIN // this is the AdderError event
            -----
            assert INTxPLS signal, if AdderError interrupts are enabled:
            GOTO PTO Disabled state; // disable the PLS block now
            -----
        END
        ENDIF
    -----
    END
    ENDIF
    set cycle time counter = 0.
    -----
END
ENDIF

IF (cycle time counter >= (1/2 * cycle time preset)) THEN
    PLSxOUT = 0;
ELSE // output still in logic high portion of the current cycle
    PLSxOUT = 1;
ENDIF

```

Figure 16

1700

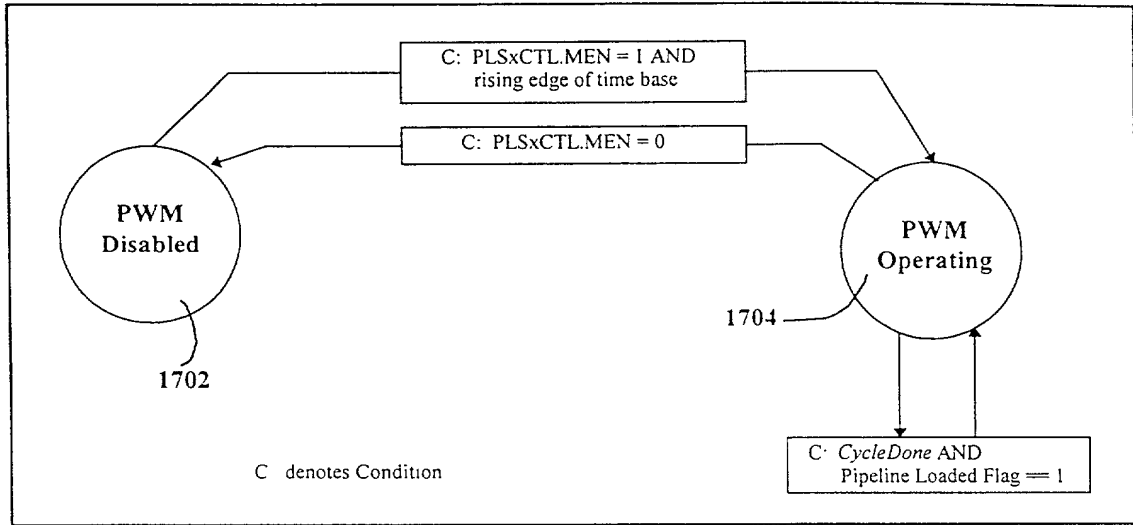


Figure 17

```

cycle time counter = cycle time counter + 1;
IF (cycle time counter >= cycle time preset) THEN
BEGIN // this is the CycleDone event
    -----
    IF (pipeline loaded flag is set) THEN
    BEGIN
        -----
        transfer values from pipeline registers into operating registers;
        clear pipeline loaded flag;
        -----
    END
    ENDIF
    set cycle time counter = 0;
    -----
END
ENDIF

IF (cycle time counter >= (pulse width preset)) THEN
    PLSxOUT = 0;
ELSE // output still in logic high portion of the current cycle
    PLSxOUT = 1;
ENDIF

```

Figure 18

HIGH SPEED OPERATIONS				VALID OPERANDS
Instruction	Mnemonic & Operand(s)	Description	STL Status Element	
Pulse Train Output Profile	PTOP t, n	When S0 = 1, the PTO profile specified in the table for output n is executed. ENO ← S0 * /e	STK, <current step>	Enable: S0 Table: VB, IB, QB, MB, (UI) SMB, SB, LB, *VD, *AC Output: KW (UI) 0 - 1

Definition of the TABLE for PTOp:

Byte Offset	Segment	Description of Table Entries
0		Number of profile segments (40 segments maximum)
1		Current step number being executed
2	#1	Number of steps (4 steps minimum)
4		Starting cycle time for this segment (2 to 65535 μ sec)
6		Change in cycle time per step (signed value) (0 to 65535 μ sec)
8	#2	Number of steps (4 steps minimum)
10		Starting cycle time for this segment (2 to 65535 μ sec)
12		Change in cycle time per step (signed value) (0 to 65535 μ sec)
:	:	:
:	:	:

Figure 19

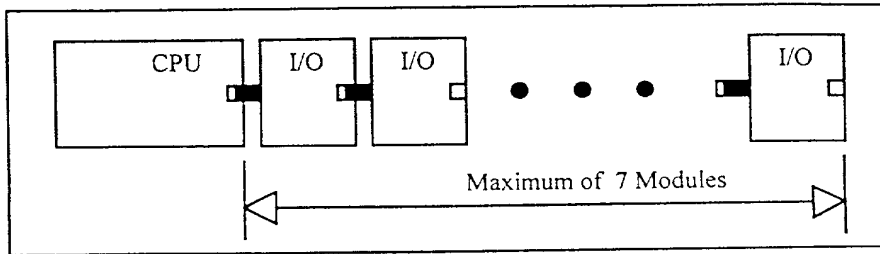


Figure 20

Signal Name	Use
EMD	Expansion Module Data - a bi-directional signal used to communicate the address and data to and from the module.
EMC[1:0]	Expansion Module Clocks - One clock is used to access expansion I/O external to the PLC, while the other is used to access I/O that is local to the PLC that does not connect directly to the ASIC.
XA_OD	Address/Output Disable - a dual function signal used to reset the state machine in the modules on the first clock of each access cycle (active low) and used to indicate output disable when a fatal error has been detected (active low for an RC time constant).
EMDDIR	Expansion Module Data Direction - this signal indicates the direction of data flow on the EMD signal line. 0 - Data is driven by the module to the PLC 1 - Data is driven by the PLC to the module
EMA[2:0]	Expansion Module Address - these signals are daisy chained from PLC to module to module. The value input to a module becomes that module's address. The module will output its address plus one to the next module. The PLC drives these signals to 0 so that the module connected to the PLC has the address of 0.
+5V	5 volt power supply - Two signals carry +5 volts.
GND	Power supply return - Two signals carry ground.

Figure 21

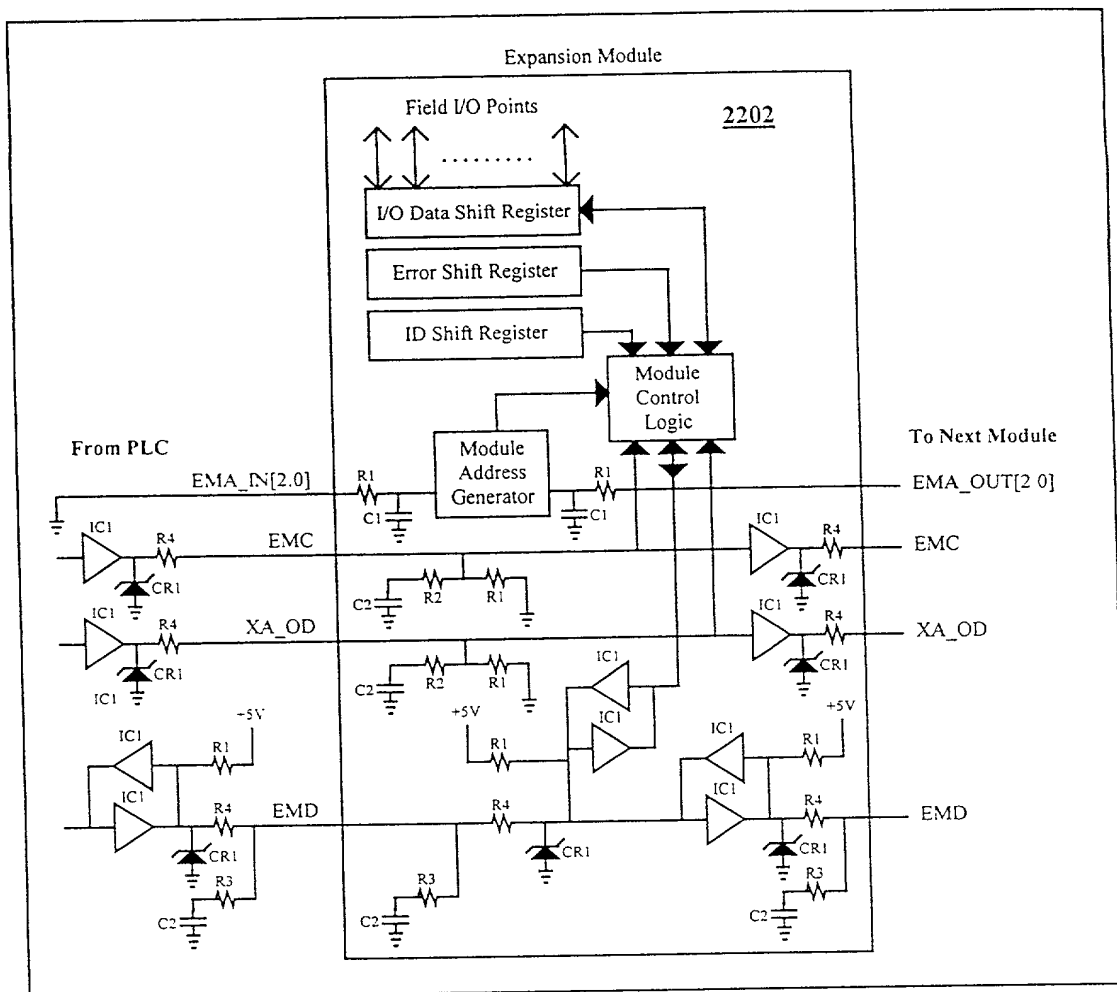


Figure 22

Reference Designator	Component Value/Type	Component Description
IC1	74ABT125/74ABT126	Tri-state buffer
CR1	TVS 5.6V Zener	Diode
R1	4.7K ohm	Resistor
R2	110 ohm	Resistor
R3	220 ohm	Resistor
R4	22 ohm	Resistor
C1	0.1 μ F	Capacitor
C2	100pF	Capacitor

Figure 23

Signal Name	Driving Device	Drive Levels				Receive Levels	
		V _{OL} (Volts) (Max)	I _{OL} (mA) (Min)	V _{OH} (Volts) (Max)	I _{OH} (mA) (Min)	V _{IL} (Volts) (Max)	V _{IH} (Volts) (Min)
EMA[2:0]	Module	0.5	3.0	2.4	-3.0	0.8	2.0
XA_OD	CPU	0.55	64.0	2.0	-32.0	0.8	2.0
EMC	CPU	0.55	64.0	2.0	-32.0	0.8	2.0
EMD	CPU	0.55	64.0	2.0	-32.0	0.8	2.0
	Module	0.55	64.0	2.0	-32.0	0.8	2.0

Figure 24

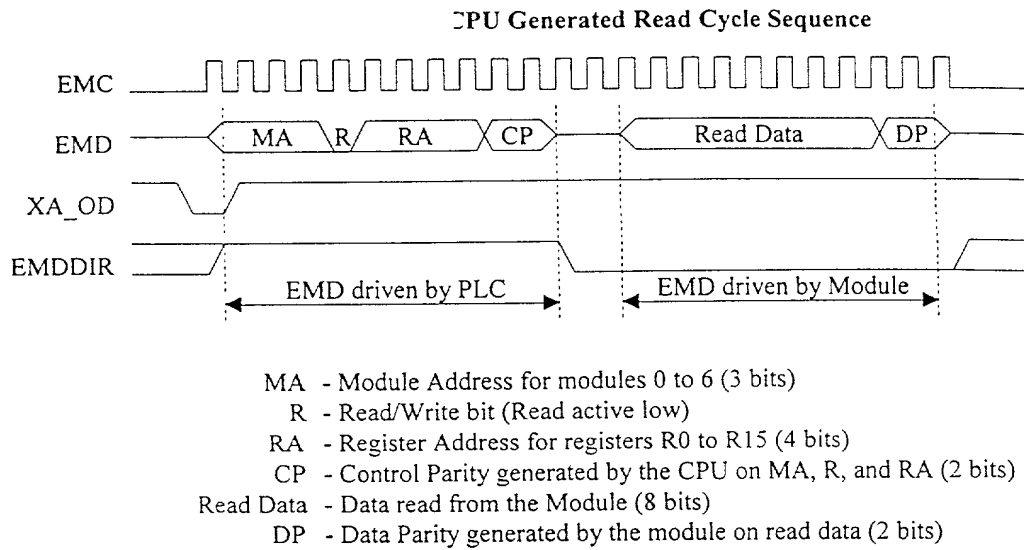


Figure 25

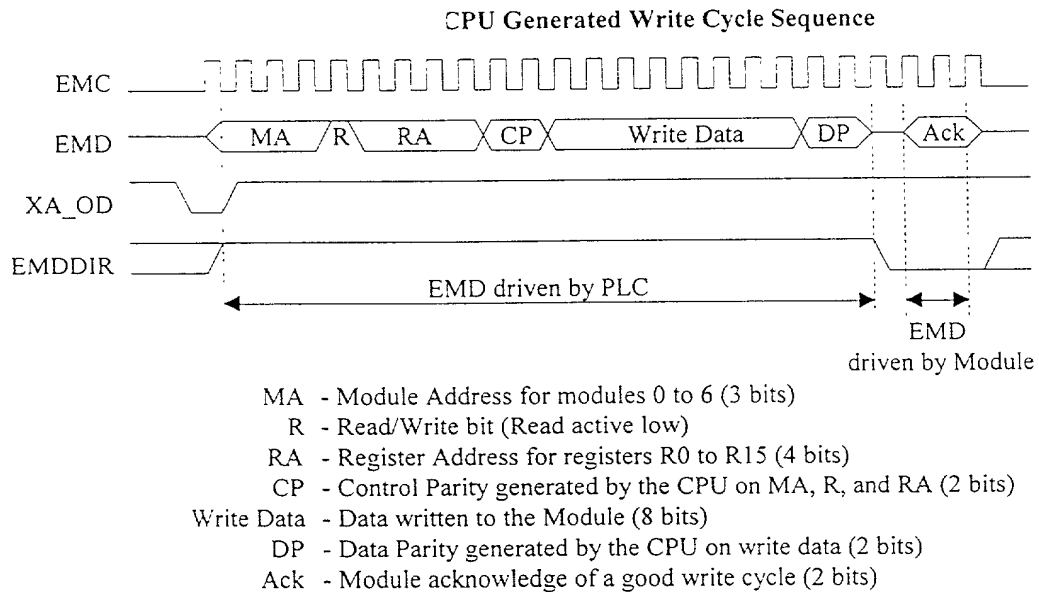


Figure 26

	<i>a</i>	<i>b</i>	<i>c</i>	<i>d</i>	<i>e</i>
P0	bit 0	bit 2	bit 4	bit 6	bit 7
P1	bit 1	bit 2	bit 3	bit 5	bit 7
5 bit odd parity = ! ((<i>a</i> xor <i>b</i>) xor (<i>c</i> xor <i>d</i>)) xor <i>e</i>)					

Figure 27

PLC Type	Port 0	Port 1
CPU 212	256	-
CPU 214	256	-
CPU 215/216	256	256

Figure 28

INTERRUPTS				
Instruction	Mnemonic & Operand(s)	Description	STL Status Elements	VALID OPERANDS
Pass Token	PASS	User program has completed its use of the token hold period and is returning control to the system.	STK	

Figure 29

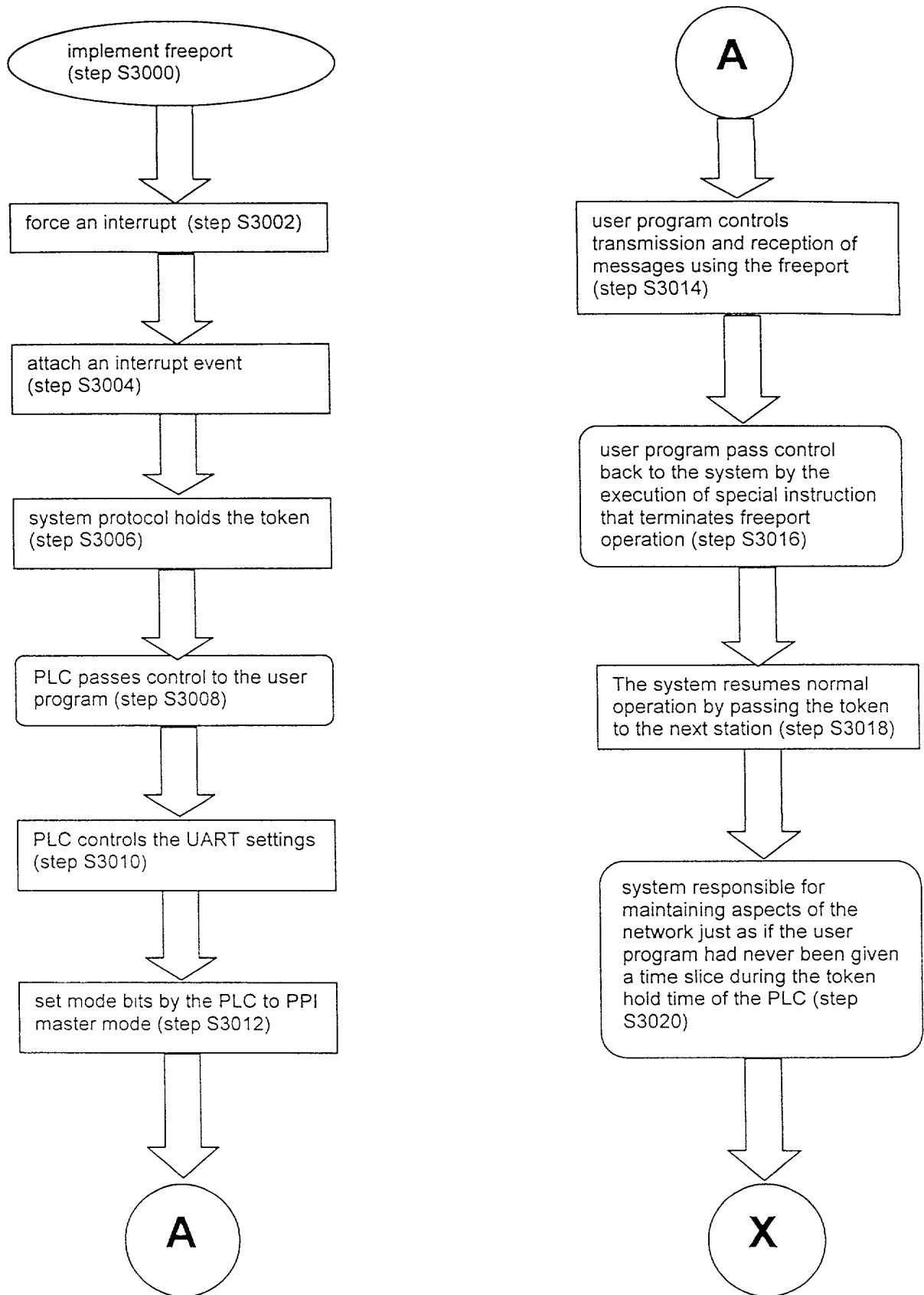


Figure 30a

SM Bit Definition (Read/Write)			
SM Bits	Description		
SM30	Port 0: Communication port usage		
	<div><div>MSB</div><div>7</div><div>LSB</div><div>0</div></div> <div>SMB30<div><div>p</div><div>p</div><div>d</div><div>r</div><div>r</div><div>r</div><div>m</div><div>m</div></div></div>		
	pp (Parity)	d (Data bits/char)	rrr (Baud Rate) mm (Protocol)
	'00' - no parity	'0' - 8 bits/char	'000' - 38,400 '00' - PPI Slave (default)
	'01' - even parity	'1' - 7 bits/char	'001' - 19,200 '01' - Freeport
	'10' - no parity		'010' - 9600 '10' - PPI Master
	'11' - odd parity		'011' - 4800 '11' - reserved (PPI Slave)
			'100' - 2400
			'101' - 1200
			'110' - 600
			'111' - 300
	When the user selects the code mm = 10 (PPI Master), the PLC will become a master on the network allowing the NETR and NETW instructions to be executed. Bits 2 through 7 are ignored in PPI modes. In PPI Master mode with the token acquired interrupt enabled, these bits are used to setup the UART prior to transferring control to the user's program.		
SM130	Port 1: Communication port usage (CPU 216 only)		
	<div><div>MSB</div><div>7</div><div>LSB</div><div>0</div></div> <div>SMB130<div><div>p</div><div>p</div><div>d</div><div>r</div><div>r</div><div>r</div><div>m</div><div>m</div></div></div>		
	pp (Parity)	d (Data bits/char)	rrr (Baud Rate) mm (Protocol)
	'00' - no parity	'0' - 8 bits/char	'000' - 38,400 '00' - PPI Slave (default)
	'01' - even parity	'1' - 7 bits/char	'001' - 19,200 '01' - Freeport
	'10' - no parity		'010' - 9600 '10' - PPI Master
	'11' - odd parity		'011' - 4800 '11' - reserved (PPI Slave)
			'100' - 2400
			'101' - 1200
			'110' - 600
			'111' - 300
	When the user selects the code mm = 10 (PPI Master), the PLC will become a master on the network allowing the NETR and NETW instructions to be executed. Bits 2 through 7 are ignored in PPI modes. In PPI Master mode with the token acquired interrupt enabled, these bits are used to setup the UART prior to transferring control to the user's program.		

Figure 30b

SM Bit Definition (Read/Write) (continued)	
SM Bits	Description
SM87	<p>Port 0: Receive message control byte. (CPU 212/214/216)</p> <div style="text-align: center;"> <div>MSB</div> <div>7</div> <div>en</div> <div>sc</div> <div>ec</div> <div>il</div> <div>c/m</div> <div>tmr</div> <div>bk</div> <div>0</div> <div>LSB</div> <div>0</div> </div> <p>en: Enable/disable receive message bit is checked each time the RCV instruction is executed. If this bit is a "0", then the receive message function is disabled. If this bit is a "1", then the receive message function is enabled.</p> <p>sc: 0 - ignore SMB88; 1 - use the value of SMB88 to detect start of message</p> <p>ec: 0 - ignore SMB89; 1 - use the value of SMB89 to detect end of message</p> <p>il: 0 - ignore SMW90; 1 - use the value of SMW90 to detect an idle line condition¹</p> <p>c/m: 0 - use timer as an inter-character timer; 1 - use timer as a message timer</p> <p>tmr: 0 - ignore SMW92; 1 - terminate receive if the time period in SMW92 is exceeded</p> <p>bk: 0 - ignore break conditions; 1 - use break condition as start of message detection</p> <p>¹By setting the sc and bk bits to 0 and the en, il, c/m and tmr bits to 1 with an idle line timer value of zero, SMW92 will be used to time out the RCV instruction without receiving any characters. If the timer is not used (tmr = 0), then any character received will be used as start of message.</p> <p>The bits of the message interrupt control byte are used to define the criteria by which the message is identified. Both start of message and end of message criteria are defined. To determine the start of a message either of two sets of logically Anded start of message criteria must be true and must occur in sequence (idle line followed by start character or break followed by start character). To determine the end of a message the enabled end of message criteria are logically ORed. The equations for start and stop criteria are given below:</p> $\text{Start of Message} = \text{il} * \text{sc} + \text{bk} * \text{sc}$ $\text{End of Message} = \text{ec} + \text{tmr} + \text{maximum character count reached}$ <p>Note: Receive will automatically be terminated by an overrun or a parity error (if enabled).</p>
SM88	Port 0: Start of message character. (CPU 212/214/216)
SM89	Port 0: End of message character. (CPU 212/214/216)
SM90 SM91	Port 0: Idle line time period given in milliseconds. The first character received after the idle line time has expired is the start of a new message. SM90 is MSB. (CPU 212/214/216)
SM92 SM93	Port 0: Inter-character/message timer timeout value given in milliseconds. If the time period is exceeded, the receive message is terminated. SM92 is MSB. (CPU 212/214/216)
SM94	Port 0: Maximum number of characters to be received (1 to 255 bytes) (CPU 212/214/216)

Figure 30c

SM Bit Definition (Read/Write) (continued)	
SM Bits	Description
SM187	<p>Port 1: Message interrupt control byte (CPU 216 only)</p> <div style="text-align: center;"> <div>MSB</div> <div>7</div> <div>en</div> <div>sc</div> <div>ec</div> <div>il</div> <div>c/m</div> <div>tmr</div> <div>bk</div> <div>0</div> <div>LSB</div> <div>0</div> </div> <p>en: Enable/disable receive message bit is checked each time the RCV instruction is executed. If this bit is a "0", then the receive message function is disabled. If this bit is a "1", then the receive message function is enabled.</p> <p>sc: 0 - ignore SMB188; 1 - use the value of SMB188 to detect start of message</p> <p>ec: 0 - ignore SMB89; 1 - use the value of SMB189 to detect end of message</p> <p>il: 0 - ignore SMW190; 1 - use the value of SMW190 to detect an idle line condition¹</p> <p>c/m: 0 - use timer as an inter-character timer; 1 - use timer as a message timer</p> <p>tmr: 0 - ignore SMW192; 1 - terminate receive if the time period in SMW192 is exceeded</p> <p>bk: 0 - ignore break conditions; 1 - use break condition as start of message detection</p> <p>¹By setting the sc and bk bits to 0 and the en, il, c/m and tmr bits to 1 with an idle line timer value of zero, SMW192 will be used to time out the RCV instruction without receiving any characters. If the timer is not used (tmr = 0), then any character received will be used as start of message.</p> <p>The bits of the message interrupt control byte are used to define the criteria by which the message is identified. Both start of message and end of message criteria are defined. To determine the start of a message either of two sets of logically Anded start of message criteria must be true and must occur in sequence (idle line followed by start character or break followed by start character). To determine the end of a message the enabled end of message criteria are logically Ored. The equations for start and stop criteria are given below:</p> $\text{Start of Message} = \text{il} * \text{sc} + \text{bk} * \text{sc}$ $\text{End of Message} = \text{ec} + \text{tmr} + \text{maximum character count reached}$ <p>Note: Receive will automatically be terminated by an overrun or a parity error (if enabled).</p>
SM188	Port 1: Start of message character (CPU 216 only)
SM189	Port 1: End of message character (CPU 216 only)
SM190	Port 1: Idle line time period given in milliseconds. The first character received after the idle line time has expired is the start of a new message. SM190 is MSB. (CPU 216 only)
SM191	
SM192	Port 1: Inter-character/message timer timeout value given in milliseconds. If the time period is exceeded, the receive message is terminated. SM192 is MSB. (CPU 216 only)
SM193	
SM194	Port 1: Maximum number of characters to be received (1 to 255 bytes) (CPU 216 only)

Figure 30d

PLC Type	Port 0			Port 1		
	Number of Connections		Buffer Size	Number of Connections		Buffer Size
	Total	Reserved	(Bytes)	Total	Reserved	(Bytes)
CPU 221	4	1 - PG 1 - OP	128/256	-	-	-
CPU 222	4	1 - PG 1 - OP	128/256	-	-	-
CPU 224	4	1 - PG 1 - OP	128/256	-	-	-
CPU 226	4	1 - PG 1 - OP	128/256	4	1 - PG 1 - OP	128/256

Figure 30e

PLC Type	Port 0			Port 1		
	Number of Connections		Buffer Size	Number of Connections		Buffer Size
	Total	Reserved	(Bytes)	Total	Reserved	(Bytes)
CPU 221	4	1 - PG 1 - OP	128/256	-	-	-
CPU 222	4	1 - PG 1 - OP	128/256	-	-	-
CPU 224	4	1 - PG 1 - OP	128/256	-	-	-
CPU 226	4	1 - PG 1 - OP	128/256	4	1 - PG 1 - OP	128/256

Figure 30e

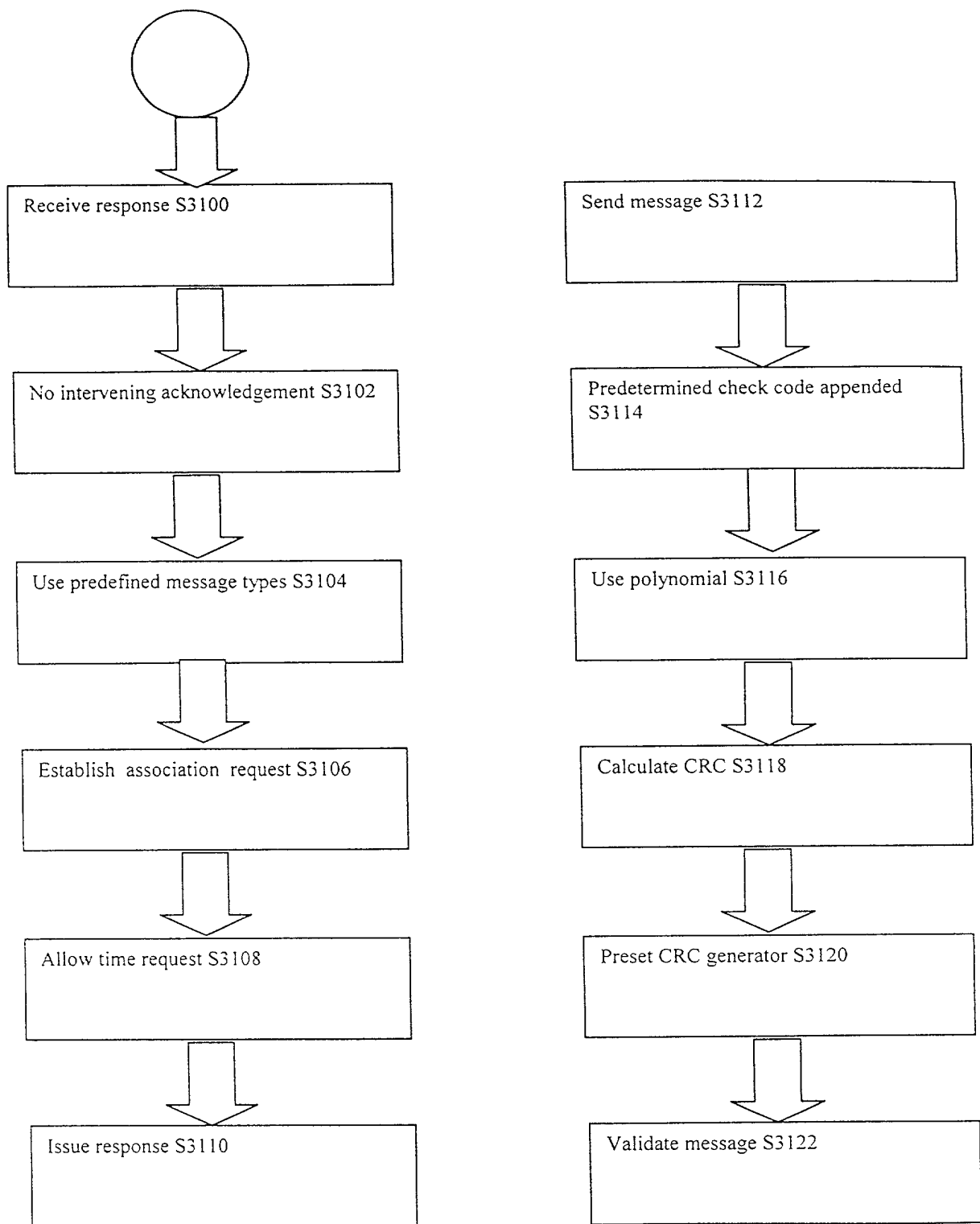


Figure 31

PROGRAM CONTROL FUNCTIONS				
Instruction	Mnemonic & Operand(s)	Description	STL Status Element	VALID OPERANDS
Hide	HIDE n, a, p	The HIDE label marks the start of a block of n instructions that are encrypted using the password, p, when a is non-zero.	STK, SMB1	Enable: None n: KW (2 bytes) (UI) a: KW (2 bytes) (UI) p: KD (4 bytes) (UI)

Figure 32a

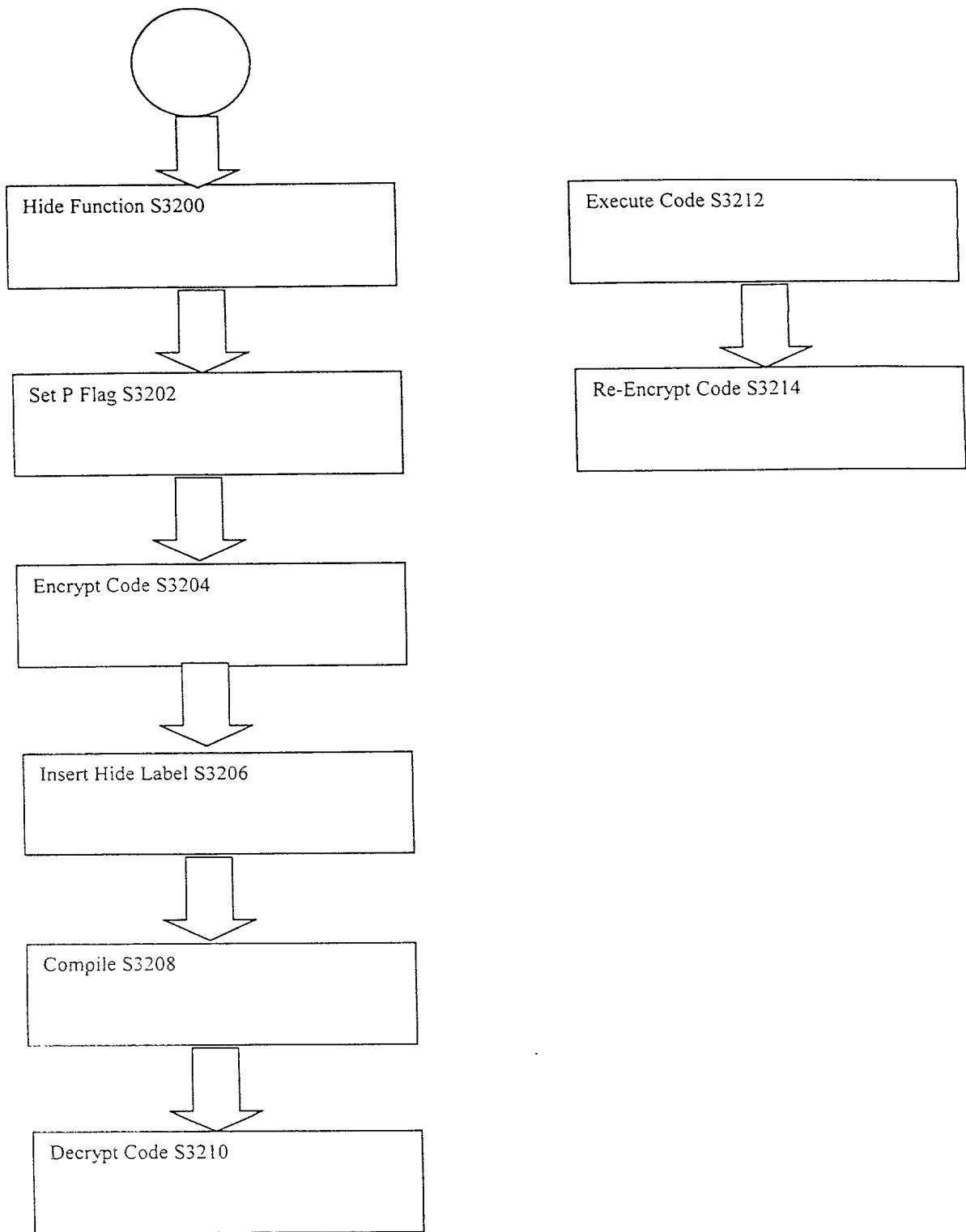


Figure 32b

PROGRAM CONTROL FUNCTIONS				
Instruction	Mnemonic & Operand(s)	Description	STL Status Element	VALID OPERANDS
System Function Call	SFC f, s, #_parms, p0, p1, p2, ...	When S0 = 1, execute the system function identified by f and the sub- function identified by s.	STK, SMB1, <p0>, <p1>, <p2>, ...	Enable: S0 f: KW (UI) 0-65536 s: KW (UI) 0-65536 #parms: KB (UI) 0-16 p0, ... : Bit, Byte, Word, Dword Bit V, I, Q, M, SM, S, T, C, L Byte VB, IB, QB, MB, SMB, SB, KB, LB Word VW, T, C, IW, QW, MW, SMW, SW, LW, KW Dword VD, ID, QD, MD, SMD, SD, HC, LD, KD, &VB, &IB, &QB, &MB, &T, &C, &SB Note: Constants and address pointer specifications are not allowed for output or input/output parameters.

Figure 33a

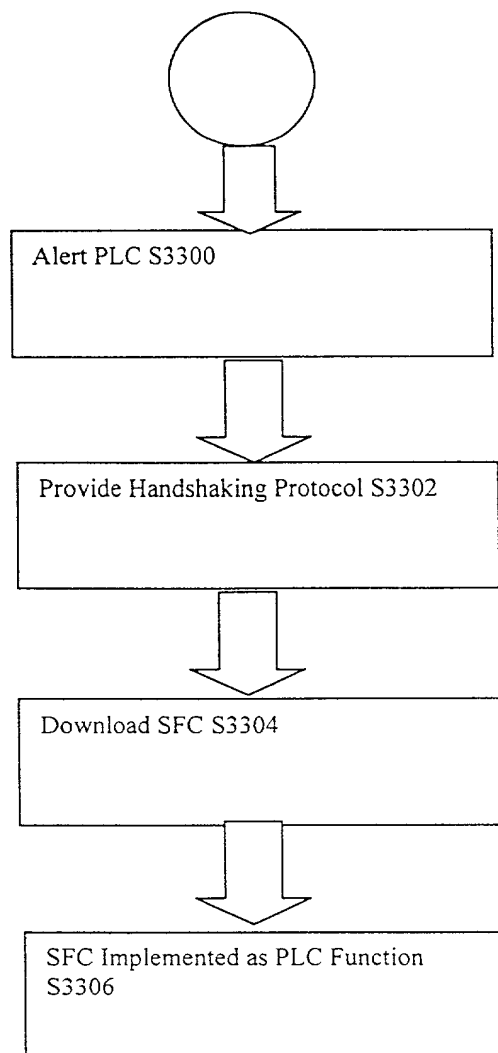


Figure 33b

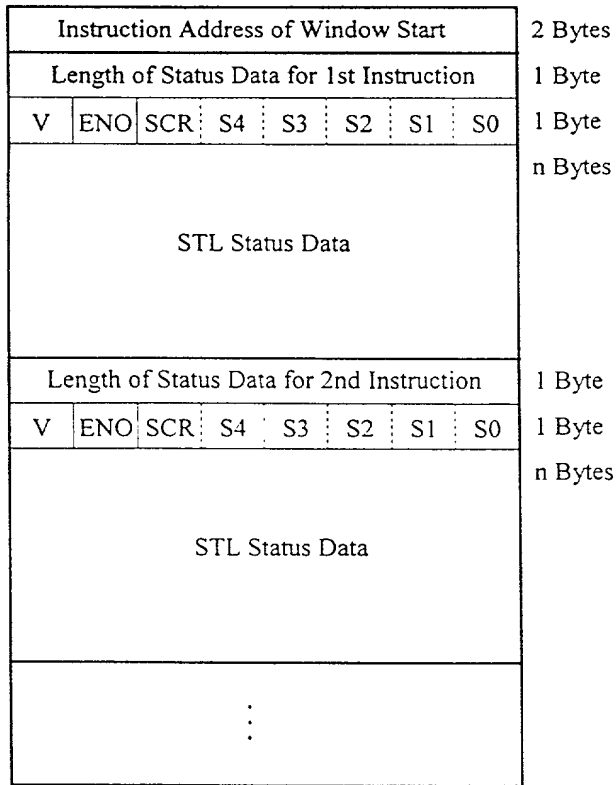


Figure 34a

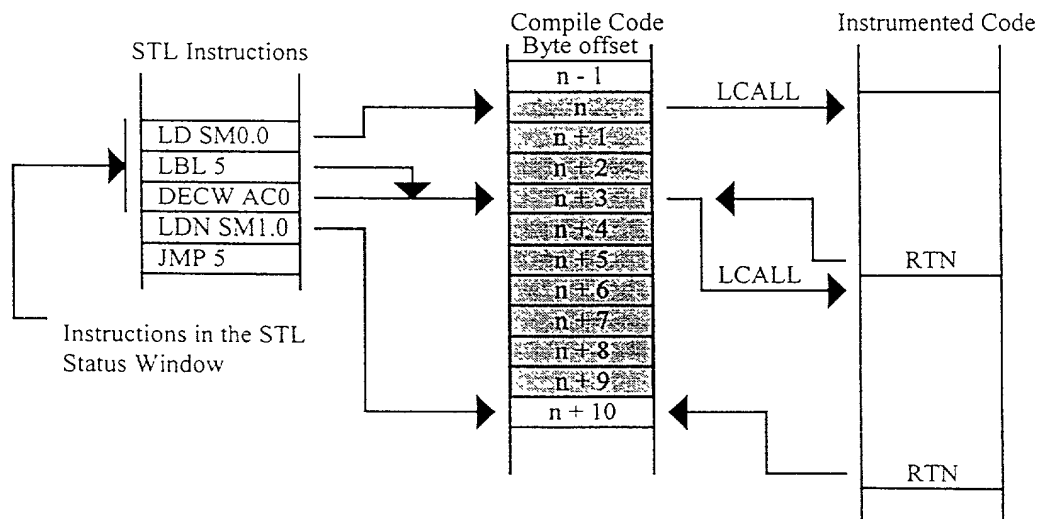


Figure 34b

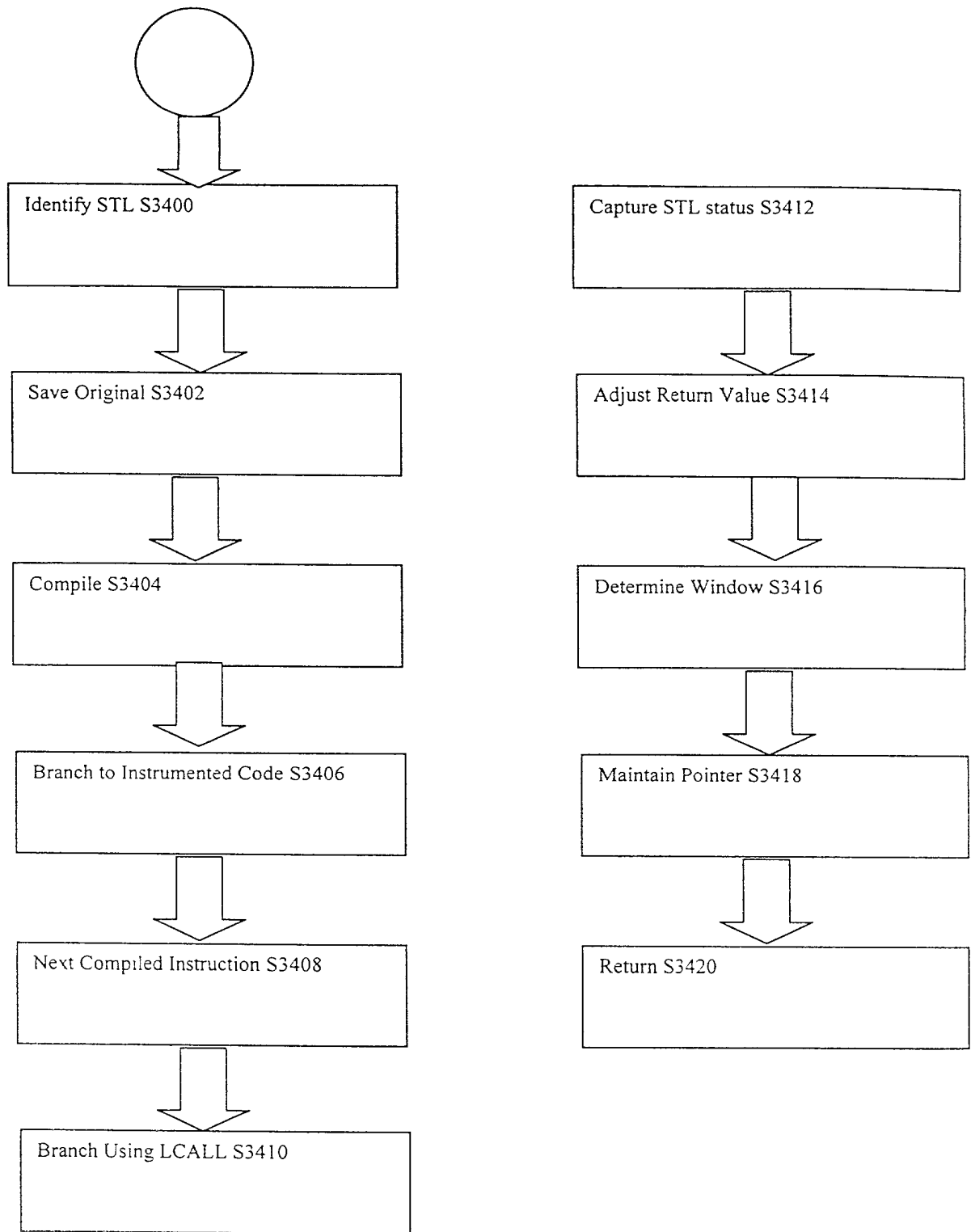


Figure 34c

	Basic Instr.	Compiled To	Bytes	Cycles
1	LD	RLC A MOV C, <bit>	1 2	1 1
2	LDN	RLC A MOV C, <bit> CPL C	1 2 1	1 1 1
3	AND	ANL C, <bit> NOP	2 1	2 1
4	ANL	ANL C, <bit> NOP	2 1	2 1
5	OR	ORL C, <bit> NOP	2 1	2 1
6	ORN	ORL C, <bit> NOP	2 1	2 1
7		MOV <bit> C NOP	2 1	2 1
8	ALD	ANL C, ACC.0 RR A	2 1	2 1
9	OLD	ORL C, ACC.0 RR A	2 1	2 1
10	NOT	CPL C NOP NOP	1 1 1	1 1 1
11	LPS	RL A MOV ACC.0, A	1 2	1 2
12	LPP	RRC A NOP NOP	1 1 1	1 1 1
13	LRD	MOV C, ACC.0	2	2
14	RET	RET NOP NOP	1 1 1	2 1 1
15	INT	CLR A NOP NOP	1 1 1	1 1 1
16	END	JNC S+0 RET	2 1	2 2
17	CRETI	JNC S+0 RET	2 1	2 2

Figure 34d

Housing	Height	Width	Depth
CPU 221	80 mm	90 mm	62 mm
CPU 222	80 mm	90 mm	62 mm
CPU 224	80 mm	120.5 mm	62 mm
CPU 226	80 mm	190 mm	62 mm
8 Point I/O Module	80 mm	46 mm	62 mm
16 Point I/O Module	80 mm	71.2 mm	62 mm
32 Point I/O Module	80 mm	125 mm	62 mm
Intelligent Module	80 mm	90 mm	62 mm

Figure 35a

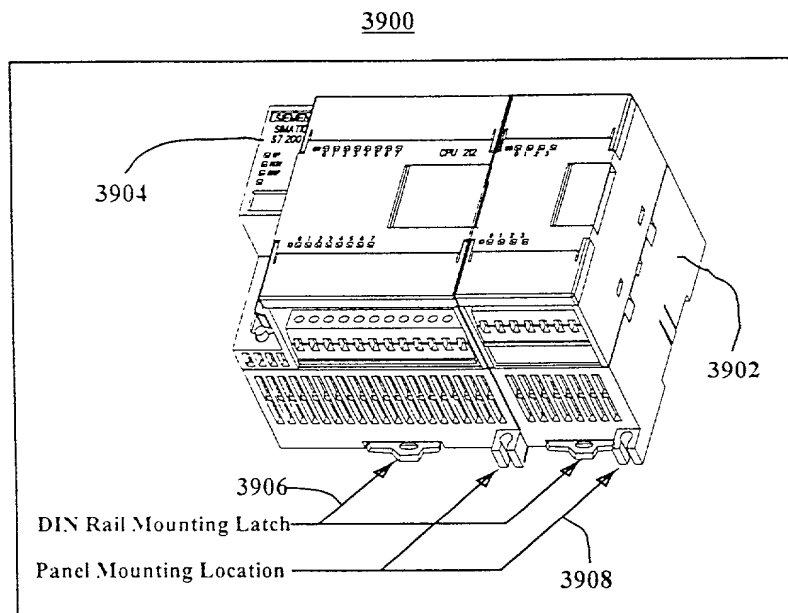
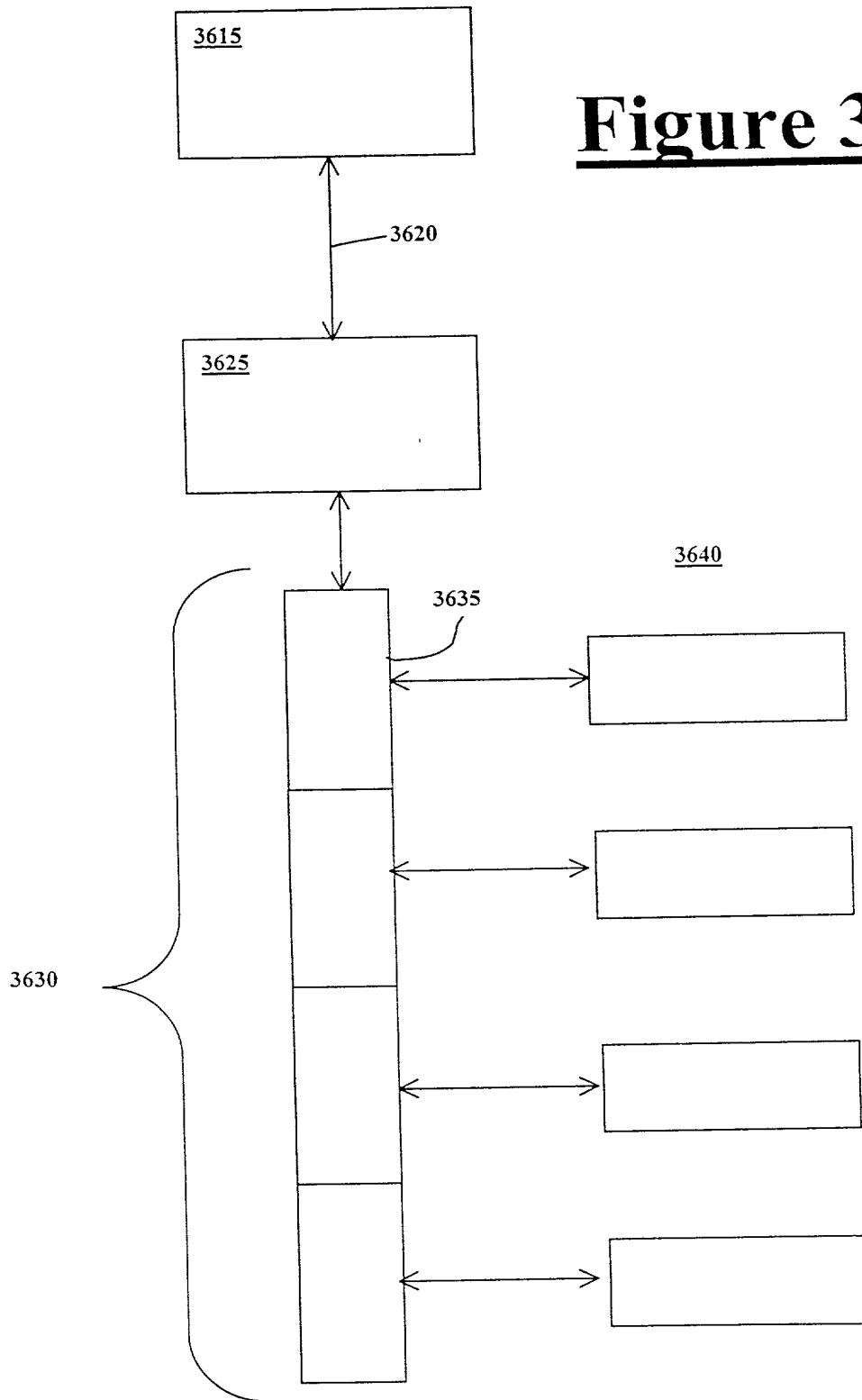


Figure 35b

3610

Figure 36



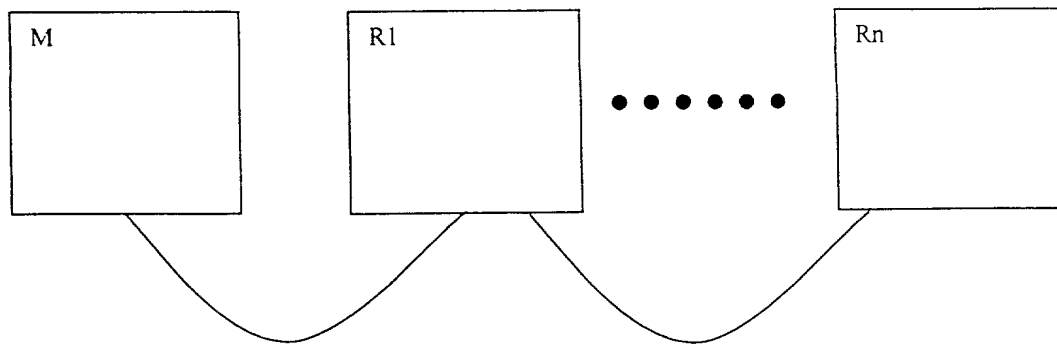


Figure 37a

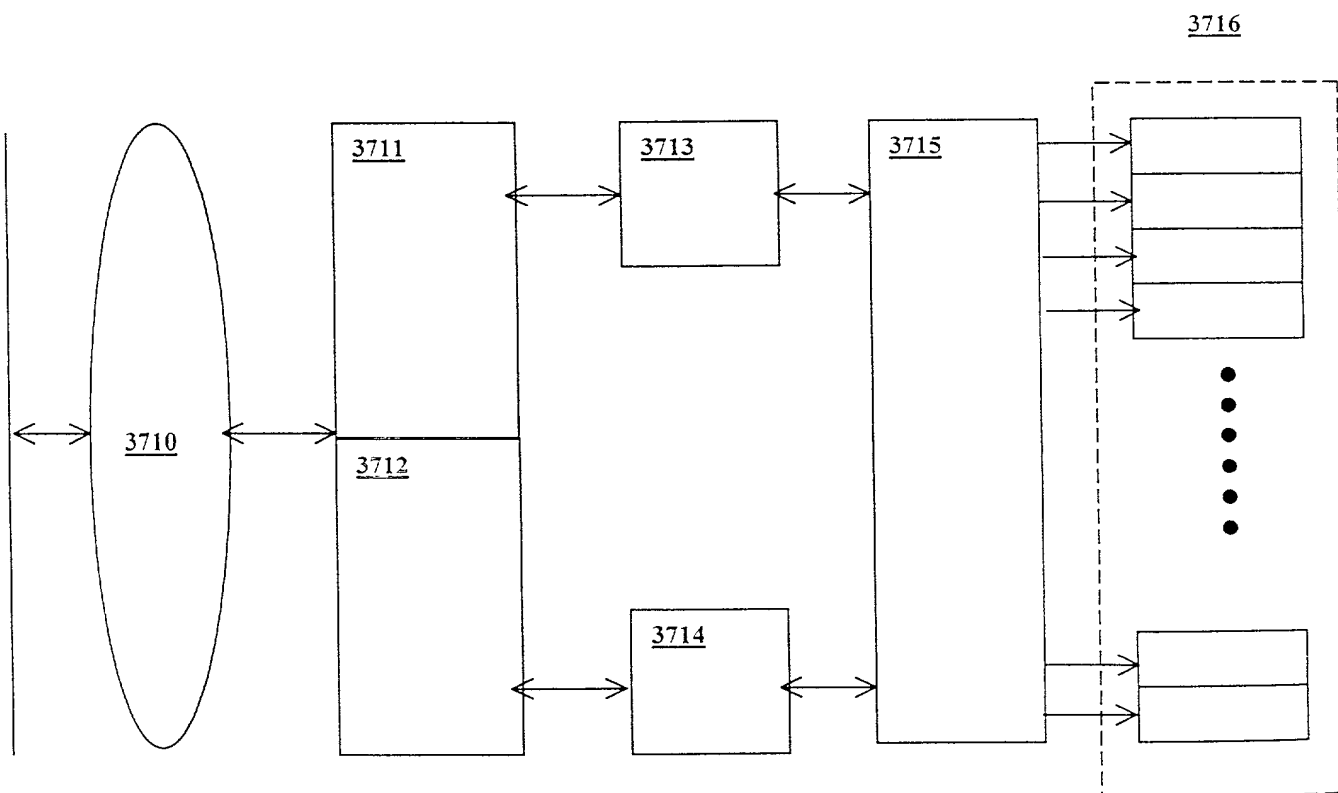
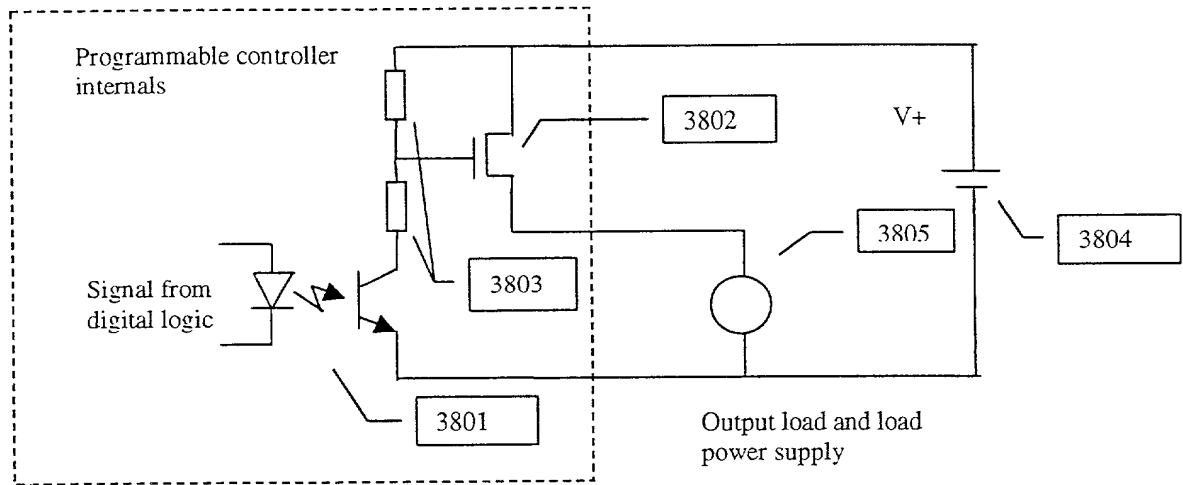


Figure 37b



**Figure 38 : Typical DC Output of Programmable Logic Controller
FET Type Sourcing Output**

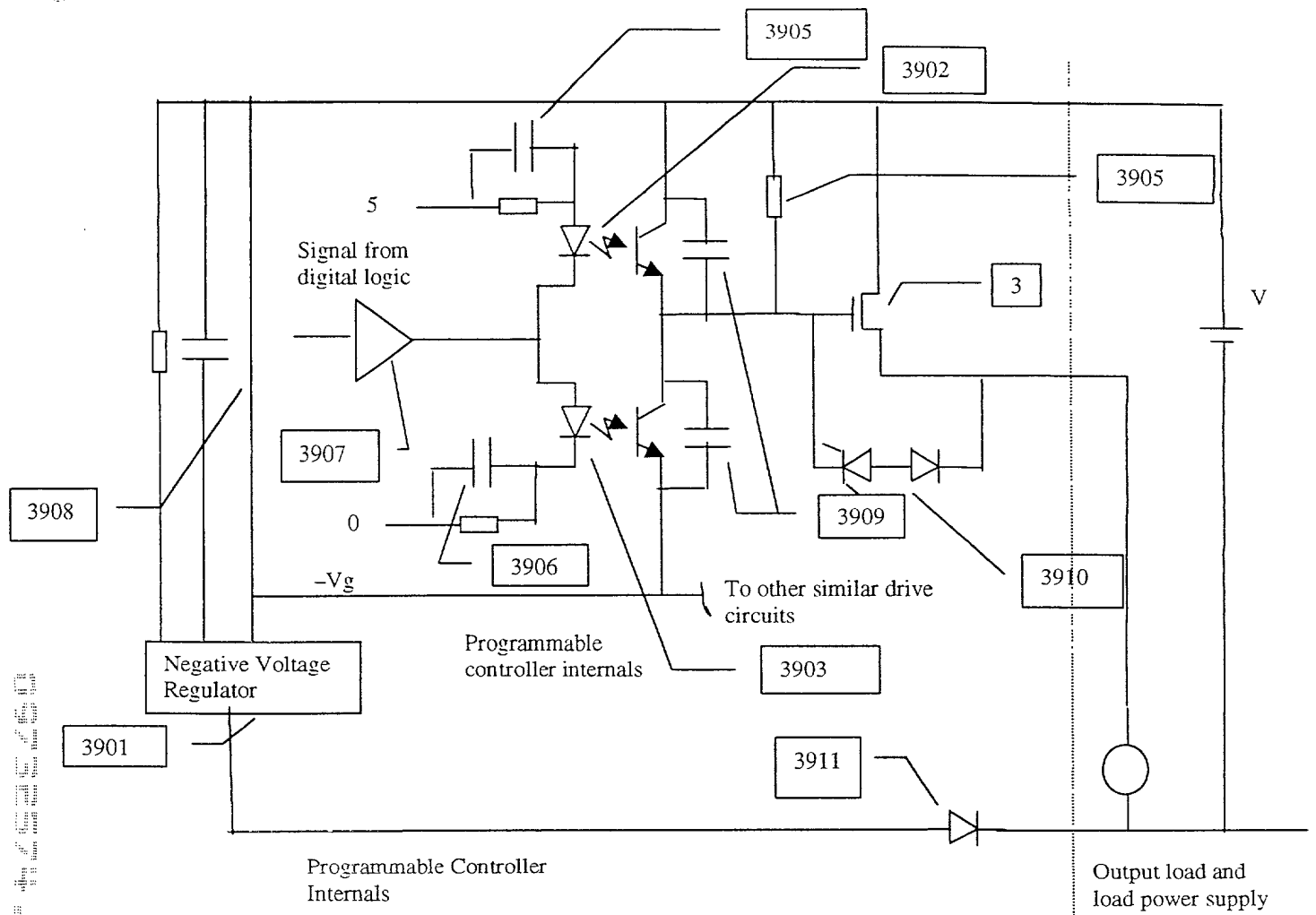


Figure 39 : High speed DC output of Programmable Logic Controller, using push-pull optocoupler circuit.